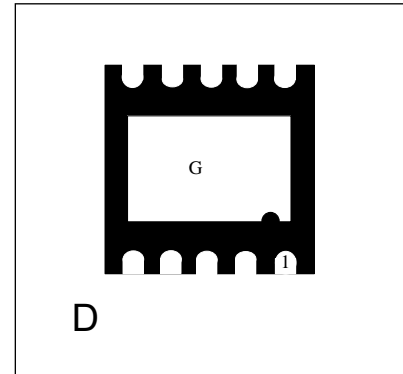




## Features

- Array of surge rated diodes with internal TVS Diode
- Small package saves board space
- Protects up to four I/O lines
- Low capacitance for high-speed interfaces
- Low leakage current and clamping voltage
- Low operating voltage: 3.3V
- Solid-state silicon-avalanche technology



## IEC Compatibility (EN61000-4)

- IEC 61000-4-2 (ESD)  $\pm 30\text{kV}$  (air),  $\pm 30\text{kV}$  (contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lightning) 28A (8/20 $\mu\text{s}$ )

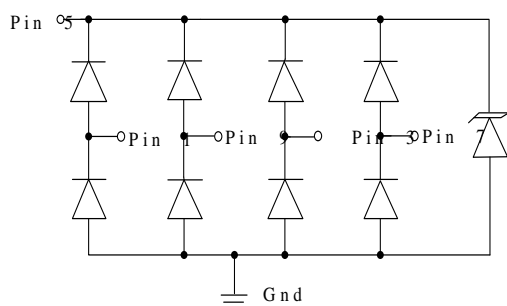
## Mechanical Characteristics

- DFN2.6x2.6-10L package (2.6 $\times$ 2.6 $\times$ 0.5mm)
- Molding compound flammability rating: UL 94V-0
- Marking: Marking Code+ Data Code
- Packaging: Tape and Reel
- RoHS Compliant

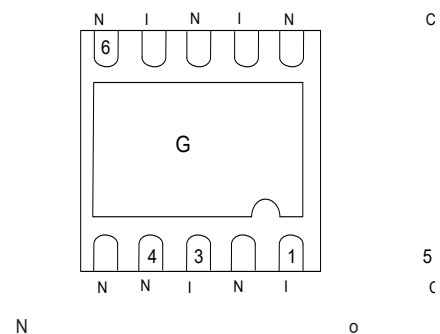
## Applications

- USB 2.0
- 10/100/1000 Ethernet
- Digital Visual Interface (DVI)
- T1/E1 Secondary Protection
- T3/E3 Secondary Protection
- Analog Video

## Circuit Diagram



## Package Configuration

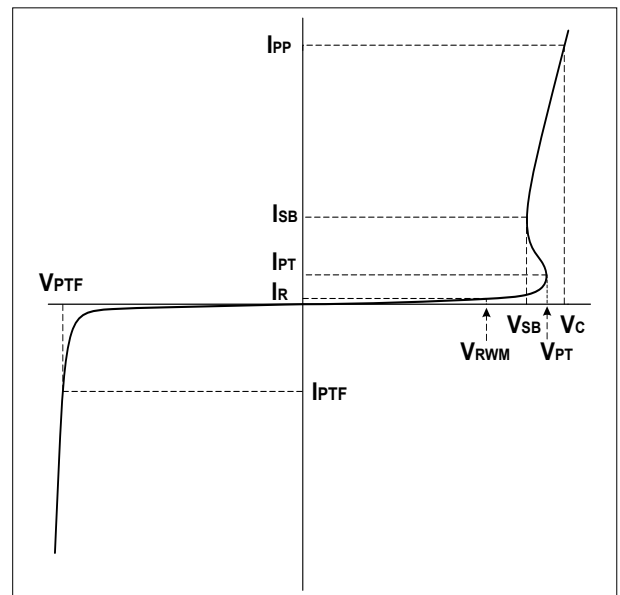


## Absolute Maximum Rating

Rating	Symbol	Value	Units
Peak Pulse Power ( $t_p = 8/20\mu s$ )	$P_{PP}$	500	Watts
Operating Temperature	$T_J$	-55 to + 125	°C
Storage Temperature	$T_{STG}$	-55 to +150	°C

## Electrical Parameters (T=25°C)

Symbol	Parameter
$I_{PP}$	Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Reverse Stand-Off Voltage
$I_R$	Reverse Leakage Current @ $V_{RWM}$
$V_{PT}$	Punch-through Breakdown Voltage @ $I_T$
$V_{SB}$	Snap-Back Voltage @ $I_{SB}$
$I_{SB}$	Snap-Back Current
$I_{PT}$	Test Current
$V_{PTF}$	Forward Punch-through Breakdown Voltage @ $I_{PTF}$
$I_{PTF}$	Forward Test Current



## Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Reverse Stand-Off Voltage	$V_{RWM}$	Any I/O pin to ground			3.3	V
Reverse Breakdown Voltage	$V_{BR}$	$I_T = 1mA$ Any I/O pin to ground	3.5			V
Snap-Back Voltage	$V_{SB}$	$I_{SB} = 50mA$ Any I/O pin to ground	2.8			
Reverse Leakage Current	$I_R$	$V_{RWM} = 3.3V, T=25°C$ Any I/O pin to ground			500	nA
Clamping Voltage	$V_C$	$I_{PP} = 28A, t_p = 8/20\mu s$ Any I/O pin to ground		14	18	V
ESD Clamping Voltage <sup>1</sup>	$V_C$	$I_{PP} = 4A$ $t_p = 0.2/100ns$		8.4		V
ESD Clamping Voltage <sup>1</sup>	$V_C$	$I_{PP} = 16A$ $t_p = 0.2/100ns$		11.2		V
Dynamic Resistance <sup>1,2</sup>	$R_{DYN}$	TLP=0.2/100ns		0.22		$\Omega$
Junction Capacitance	$C_j$	$V_R = 0V, f = 1MHz$ I/O pin to GND		2.7	4	pF
		$V_R = 0V, f = 1MHz$ Between I/O pins		1.3	3	pF

**Note:** 1、TLP Setting :  $t_p=100ns, t_r=0.2ns, I_{TLP}$  and  $V_{TLP}$  sample window: $t_1=70ns$  to  $t_2=90ns$ .

2、Dynamic resistance calculated from  $I_{PP}=4A$  to  $I_{PP}=16A$  using "Best Fit"

## Typical Characteristics

Figure 1: Peak Pulse Power vs. Pulse Time

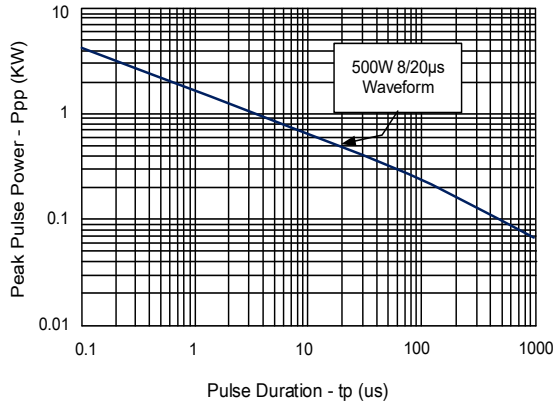


Figure 2: Power Derating Curve

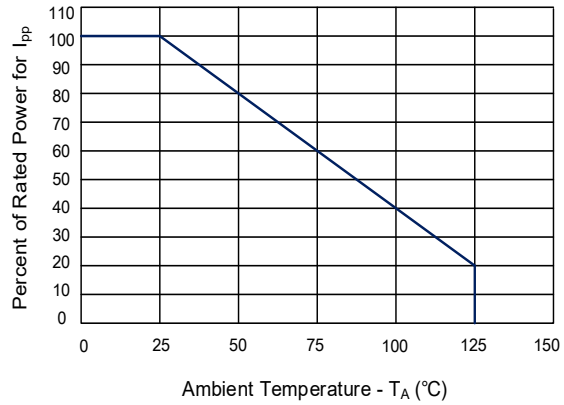


Figure 3: Clamping Voltage vs. Peak Pulse Current

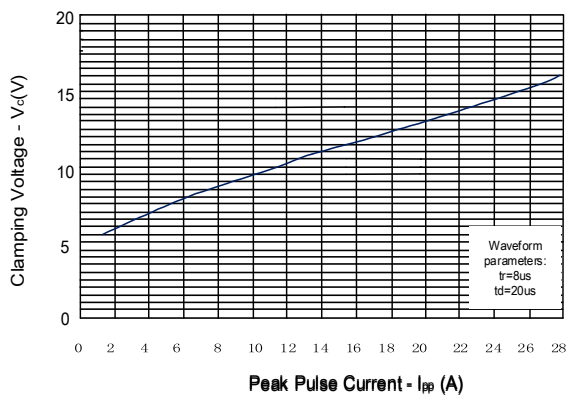


Figure 4: Capacitance vs. Reverse Voltage

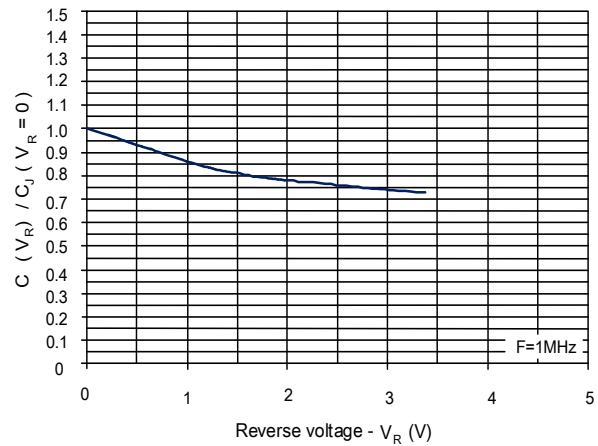


Figure 5: 8/20μs Pulse Waveform

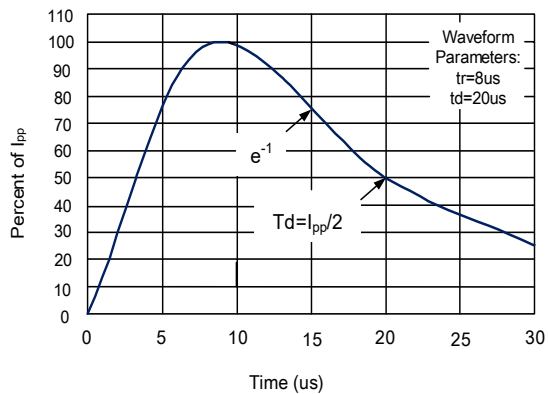
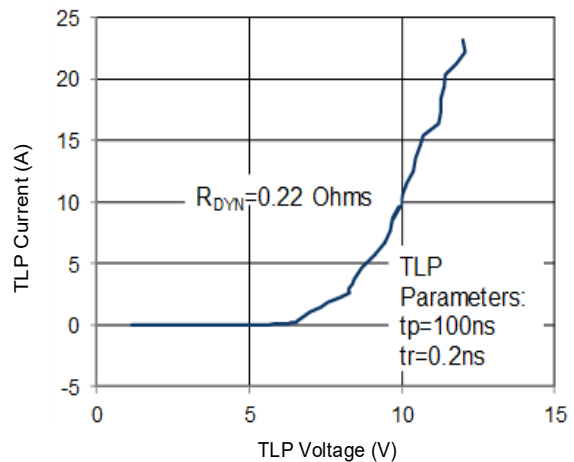


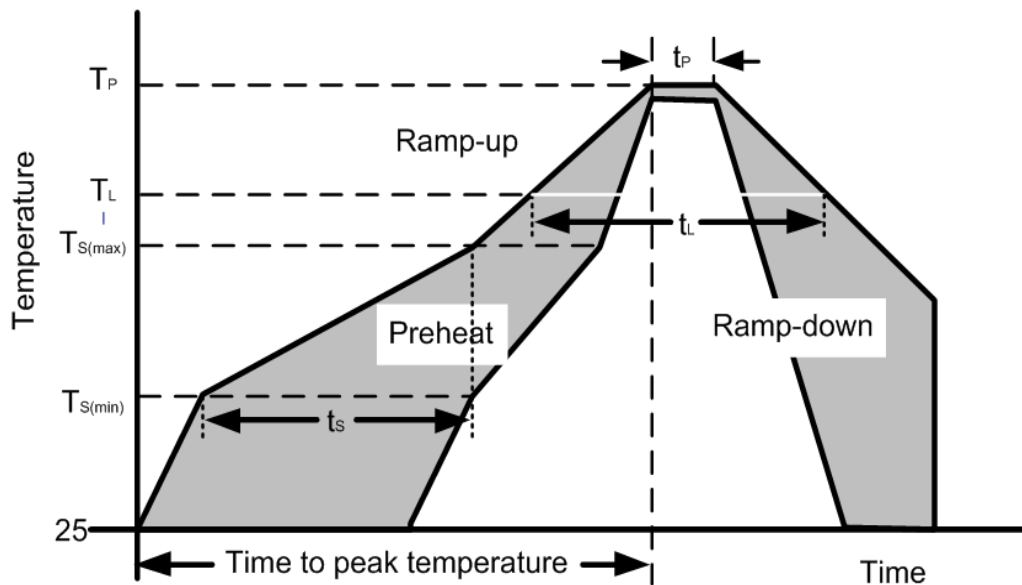
Figure 6: TLP I-V Curve



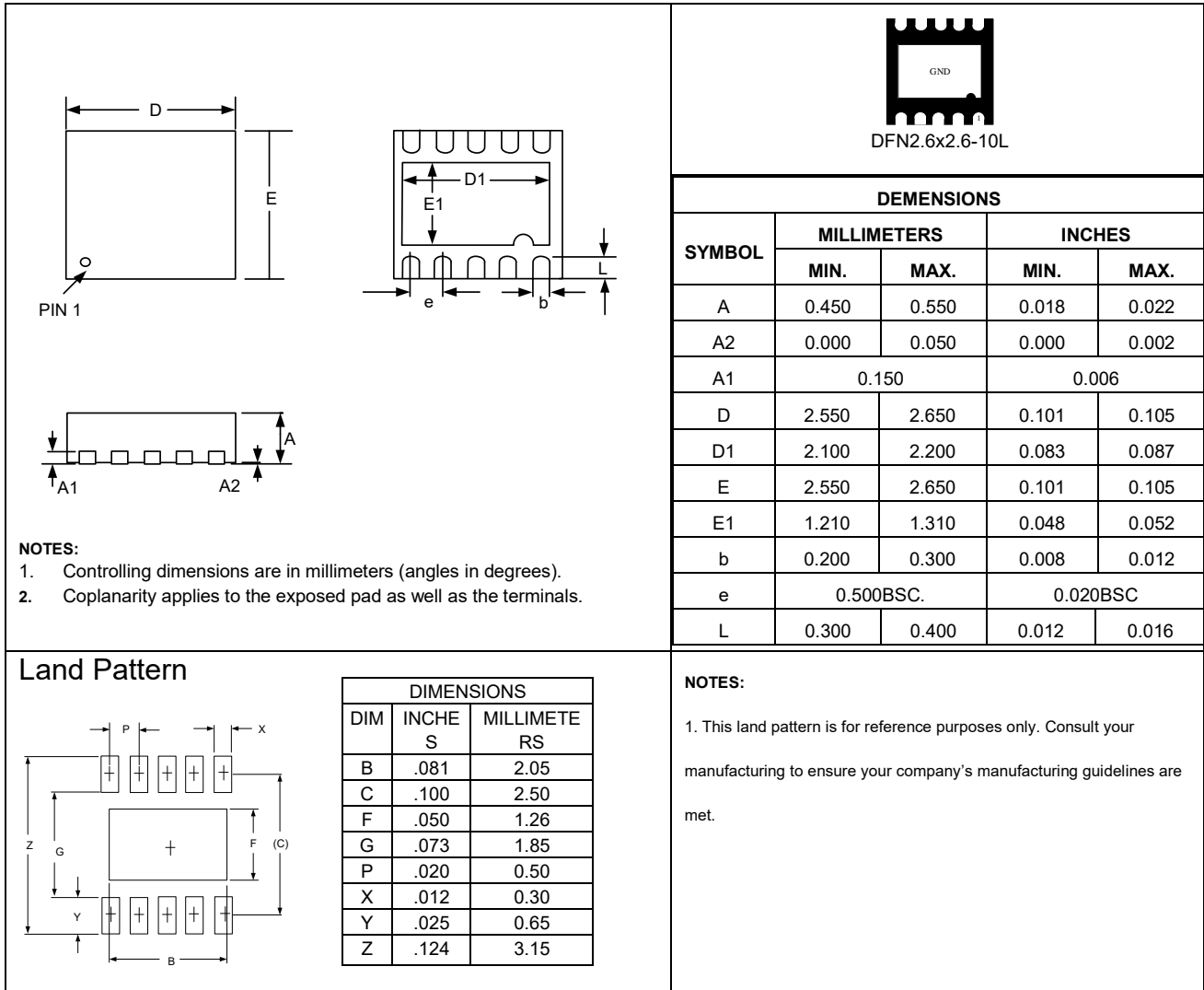


### Soldering Parameters

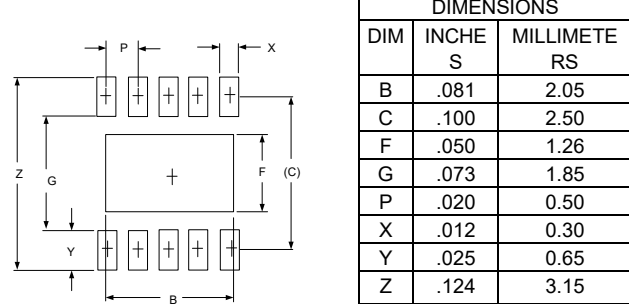
Reflow Condition		Pb – Free assembly
Pre Heat	Temperature Min ( $T_{S(min)}$ )	150°C
	Temperature Max ( $T_{S(max)}$ )	200°C
	Time (min to max) ( $t_s$ )	60 – 190 secs
Average ramp up rate (Liquidus Temp) ( $T_L$ ) to peak		5°C/second max
$T_{S(max)}$ to $T_L$ ——Ramp-up Rate		5°C/second max
Reflow	Temperature ( $T_L$ ) (Liquidus)	217°C
	Temperature ( $t_L$ )	60 – 150 seconds
Peak Temperature ( $T_P$ )		260+0/-5 °C
Time within actual peak Temperature ( $t_p$ )		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature ( $T_P$ )		8 minutes Max.
Do not exceed		280°C



## Outline Drawing –DFN2.6x2.6-10L



### Land Pattern



**NOTES:**

1. This land pattern is for reference purposes only. Consult your manufacturing to ensure your company's manufacturing guidelines are met.

## Marking Codes

Part Number	DW3.3-4R1N-S	Marking Code	2201 YYWW (YYWW: Date Code)
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## Package Information

Qty: 3k/Reel